Research

Available Online at www.ijcrr.in

International Journal of Contemporary Research and Review
CrossRefDOI: http://dx.doi.org/10.15520/ijcrr/2017/8/11/356

ISSN 0976 – 4852
November, 2017|Volume 08|Issue 11|

The Phase-Locked Loop and Costas Loop

Serkan YAKUT

Department of Electrical and Electronics Engineering, Balıkesir University, Turkey.

Accepted 2017-10 -15; Published 2017-11-04

Abstract:

In this study, the classical phase-locked loop (PLL) and Costas loop are investigated together. How the synchronization is obtained by the carrier recovery from the sinusoidal reference signal is mathematically shown with some assumptions and presented. It is concluded from this paper that Costas loop produces about half of the error signal produced by the PLL in the locked-stateoperation. This result may affect the decision whether the Costas loop will be used more frequently in the phase coherent communication systems in the future.

Keywords: Phase-locked loop, Costas loop, carrier recovery, phase coherent communication.

1. Introduction:

The PLL is a nonlinear control system with feedback loop and it may be described as that has the capability of obtaining the carrier signal frequency and the phase [1, 2].With the development of integrated circuits (ICs), PLL applications have begun to be extensively used in modern electrical and electronics engineering systems. For the past 50 years, the PLL has been contributing to the advancement of technology, particularly in the fields of communications and servo motor control systems [3]. PLLs can generally be used to demodulate a signal, track a carrier signal, synthesize a frequency, or distribute full-time clock pulses in microprocessors [4].Another PLL method is Costas loop and is currently used for wireless communications, Global Positioning Systems (GPSs), and others [5]. It is also utilized in the demodulation of the binary phase shift keying (BPSK) signals [1].

2. Mathematical Model and Analysis:

A well-known block diagram of a PLL, which is depicted in Fig.1, consists of three basic components that are a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO).PD generates an error signal that is dependent on the phase difference between the reference input and the local oscillator output.LF is a low-pass filter (LPF), suppresses noise and high frequency components. The VCO determines the oscillation frequency with dc voltage. The model block diagram of the Costas PLL is drawn in Fig. 2. The classic PLL synchronizes the reference signal with the VCO output signal. Synchronization here means that difference between the frequencies is zero or very nearly zero and the difference between the phases is zero or kept constant.

Assume that the VCO is set so that two conditions are satisfied when the control signal is zero. The first of these conditions is that the frequency of the VCO is at the carrier frequency of the incoming wave. The second is that the VCO output signal has a 90-degree phase-shift relative to the carrier wave [6].

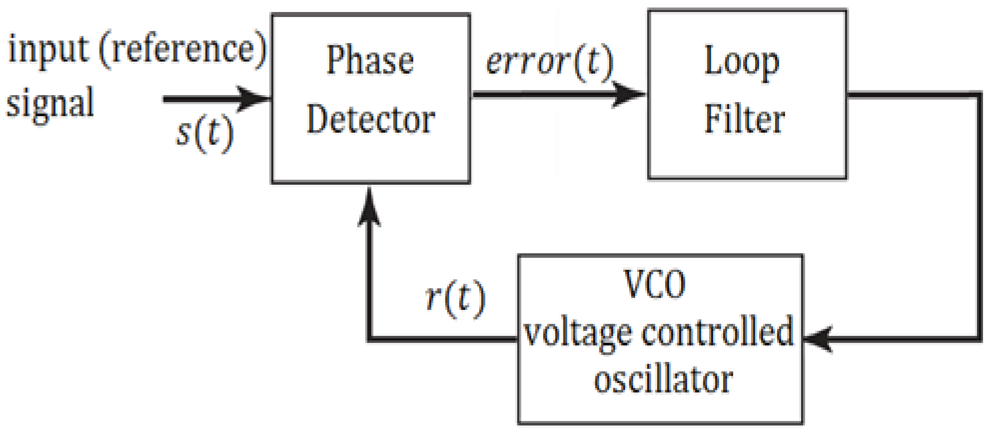

Fig.1. Block diagram of the PLL

When the input signal $s(t)$ is in the form of $\cos[4\pi f_c t + 2\phi(t)]$, $r(t)$ can be written as $\cos[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$according to the second condition previously described for the VCO. Thus, the error signal is

$$error(t) = s(t) \cdot r(t)$$

$$= \frac{1}{2}\cos[2\phi(t) - 2\hat{\phi}(t) - \pi/2] + \text{high frequency components}$$

$$\triangleq \frac{1}{2}\cos[2\phi_e(t) - \pi/2]$$

$$\triangleq \frac{1}{2}\sin[2\phi_e(t)] \qquad (1)$$

When the input signal is in the form of $\sin[4\pi f_c t + 2\phi(t)]$, the VCO output can be expressed as $\sin[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$. Hence, the error signal is defined as

$$error(t) = s(t) \cdot r(t)$$

$$= \frac{1}{2}\cos[2\phi(t) - 2\hat{\phi}(t) - \pi/2] + \text{high frequency components}$$

$$\triangleq \frac{1}{2}\cos[2\phi_e(t) - \pi/2]$$

$$\triangleq \frac{1}{2}\sin[2\phi_e(t)] \qquad (2)$$

Obtaining the same mathematical expression for (1) and (2) is the expected result. If we apply these input signals to Costas loop shown in Fig. 2.That is, when the first applied input signal is $\cos[4\pi f_c t + 2\phi(t)]$ and the local oscillator output signal is $\cos[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$, the generated error signal is found as follows

$$y_I(t) = \cos[4\pi f_c t + 2\phi(t)] \cdot \cos[4\pi f_c t + 2\hat{\phi}(t)]$$

$$= \frac{1}{2}\cos[2\phi(t) - 2\hat{\phi}(t)] + \text{high frequency components}$$

$$= \frac{1}{2}\cos[2\phi_e(t)] + \text{high frequency components}$$

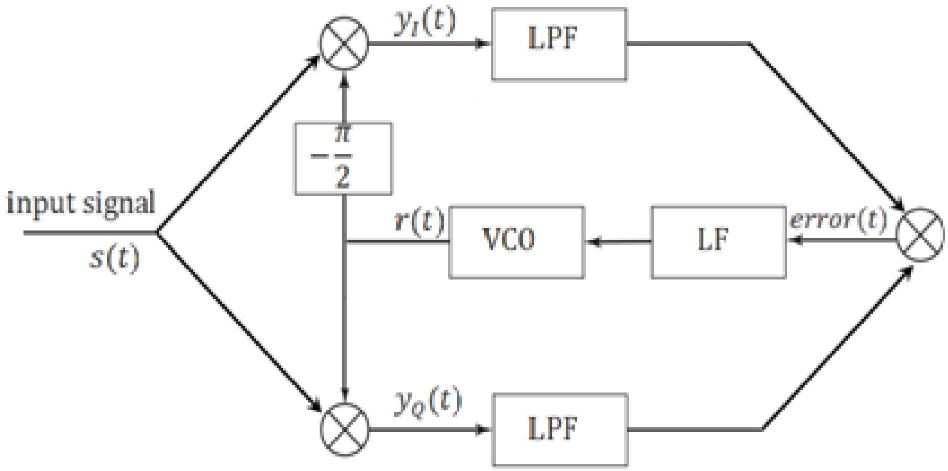

Fig. 2. Model of Costas loop

$$y_Q(t) = \cos[4\pi f_c t + 2\phi(t)] \cdot \cos[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$$

$$= \frac{1}{2}\cos[2\phi(t) - 2\hat{\phi}(t) - \pi/2] + \text{high frequency components}$$

$$= \frac{1}{2}\cos[2\phi_e(t) - \pi/2] + \text{high frequency components}$$

$$error(t) = \frac{1}{2}\cos[2\phi_e(t)] \cdot \frac{1}{2}\cos[2\phi_e(t) - \pi/2]$$

$$= \frac{1}{8}\cos[4\phi_e(t) - \pi/2]$$

$$= \frac{1}{8}\sin[4\phi_e(t)] \qquad (3)$$

When the second applied input signal is $\sin[4\pi f_c t + 2\phi(t)]$ and $r(t)$ signal is $\sin[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$, the error signal can be computed by the following equations respectively

$$y_I(t) = \sin[4\pi f_c t + 2\phi(t)] \cdot \sin[4\pi f_c t + 2\hat{\phi}(t)]$$

$$= \frac{1}{2}\cos[2\phi(t) - 2\hat{\phi}(t)] + \text{high frequency components}$$

$$= \frac{1}{2}\cos[2\phi_e(t)] + \text{high frequency components}$$

$$y_Q(t) = \sin[4\pi f_c t + 2\phi(t)] \cdot \sin[4\pi f_c t + 2\hat{\phi}(t) + \pi/2]$$

$$= \frac{1}{2}\cos\left[2\phi(t) - 2\hat{\phi}(t) - \pi/2\right] + \text{high frequency components}$$

$$= \frac{1}{2}\cos[2\phi_e(t) - \pi/2] + \text{high frequency components}$$

$$error(t) = \frac{1}{2}\cos[2\phi_e(t)] \cdot \frac{1}{2}\cos[2\phi_e(t) - \pi/2]$$

$$= \frac{1}{8}\cos[4\phi_e(t) - \pi/2]$$

$$= \frac{1}{8}\sin[4\phi_e(t)] \qquad (4)$$

Note that (3) and (4) are the same. In the phase coherent (synchronous) communications, locked-state has to be achieved and continued. The error signal in (1) can be written when the synchronization is maintained

$$error(t) \triangleq \frac{1}{2}\sin\left[2\phi(t) - 2\hat{\phi}(t)\right] = \frac{1}{2}\sin[2\phi_e(t)] \approx \phi_e(t) \qquad (5)$$

With the help of this approximation, instead of Fig. 1, we can use the linearized PLL shown in Fig. 3.

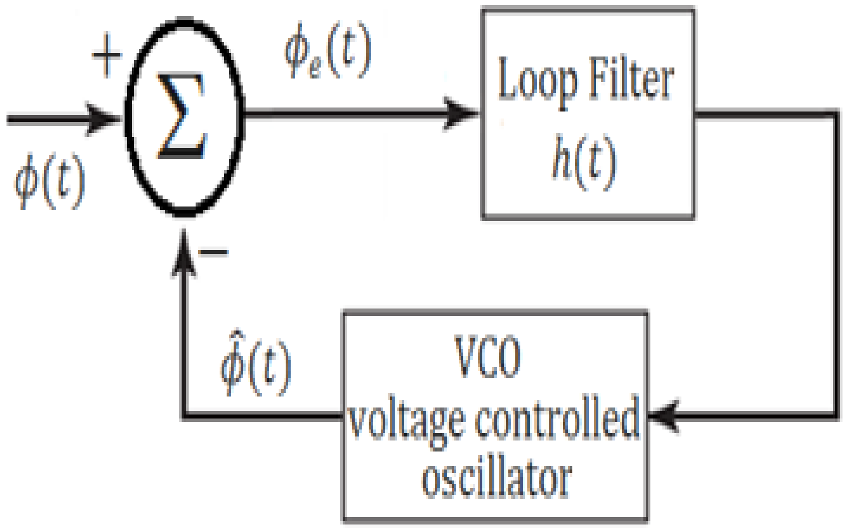

Fig. 3. Linearized PLL Model

With the same approximation, the error signal in Costas loop can be expressed again in the steady-state work (i.e. the phase difference is below 1/4 radian)

$$error(t) = \frac{1}{8}\sin\left[4\phi(t) - 4\hat{\phi}(t)\right] = \frac{1}{8}\sin[4\phi_e(t)] \approx \frac{\phi_e(t)}{2} \qquad (6)$$

The use of the mathematical approximations, it can be put forward that this value is half of the error signal in the classical PLL.

3. Conclusion:

Scientific studies on the PLL and Costas loop continue today. In the locked-state operation, it is mathematically shown that the Costas loop generates approximately half of the error signal generated by the classical PLL.This information may cause the Costas loop to be used in new applications for synchronous communication.

4. References:

[1] J. G. Proakis, M. Salehi, Digital Communications, 5th edn., NY, USA: McGraw-Hill, 2008.

[2] J. G. Proakis, M. Salehi, Fundamentals of Communication Systems, 2nd edn.,USA: Prentice Hall, 2014.

[3] G-C.Hsieh, J. C. Hung,Phase–locked loop techniques–A survey, IEEE Trans. Ind. Electron. 43 (1996) 609–615.

[4] B. B. Purkayastha, K. K. Sarma, ADigital Phase Locked Loop Based Signal and Symbol Recovery System for Wireless Channel, Springer, 2015.

[5] R. E. Best, N. V. Kuznetsov, G. A. Leonov, M. V. Yuldashev, R. V. Yuldashev, Tutorial on dynamic analysis of the Costas loop, Annual Reviews in Control, 42 (2016) 27-49.

[6] S.Haykin, M. Moher, Introduction to Analog & Digital Communications, 2nd edn., USA: Wiley, 2007.